

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K02F

High Speed Switching Applications

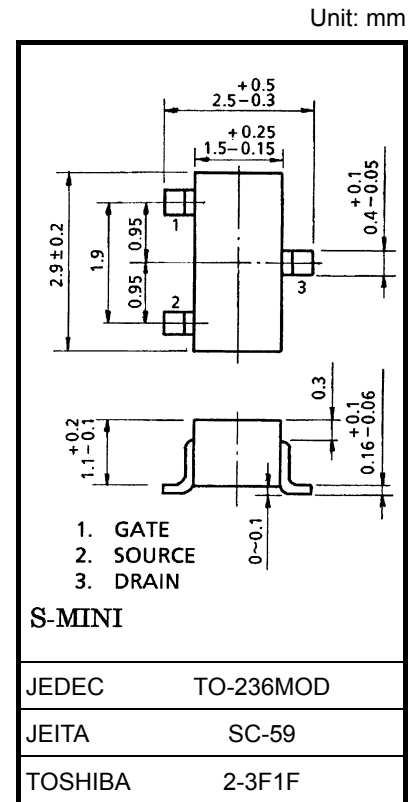
- Small package
- Low on resistance: $R_{on} = 200 \text{ m}\Omega$ (max) ($V_{GS} = 4 \text{ V}$)
 $R_{on} = 250 \text{ m}\Omega$ (max) ($V_{GS} = 2.5 \text{ V}$)
- Low gate threshold voltage: $V_{th} = 0.6 \sim 1.1 \text{ V}$ ($V_{DS} = 3 \text{ V}$, $I_D = 0.1 \text{ mA}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	± 10	V
Drain current	DC	I_D	1.0	A
	Pulse	I_{DP}	2.0	
Drain power dissipation		P_D	200	mW
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55~150	$^\circ\text{C}$

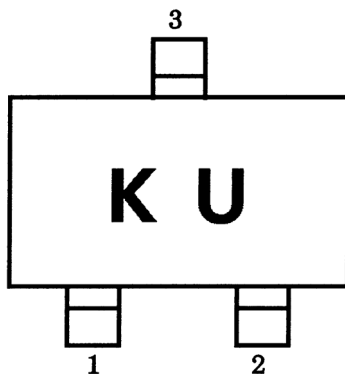
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

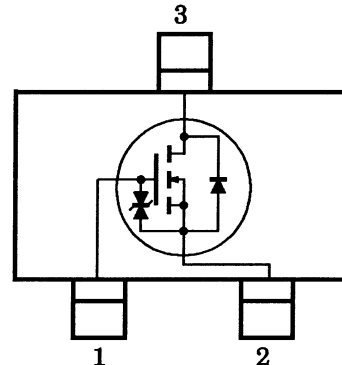


Weight: 0.012 g (typ.)

Marking



Equivalent Circuit



Handling Precaution

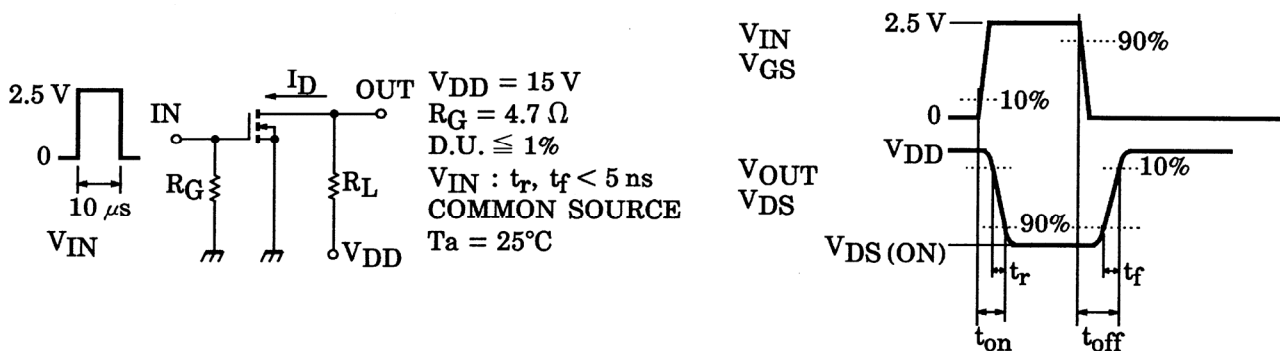
When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 10\text{ V}, V_{DS} = 0$	—	—	± 5	μA
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0$	30	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0$	—	—	1	μA
Gate threshold voltage	V_{th}	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.6	—	1.1	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 0.5\text{ A}$ (Note)	1.5	—	—	S
Drain-source ON resistance	$R_{DS(ON)}$	$I_D = 0.5\text{ A}, V_{GS} = 4\text{ V}$ (Note)	—	140	200	m Ω
		$I_D = 0.5\text{ A}, V_{GS} = 2.5\text{ V}$ (Note)	—	180	250	
Input capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	115	—	pF
Reverse transfer capacitance	C_{rss}	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	24	—	pF
Output capacitance	C_{oss}	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	60	—	pF
Switching time	Turn-on time	$V_{DD} = 15\text{ V}, I_D = 0.5\text{ A},$ $V_{GS} = 0 \sim 2.5\text{ V}, R_G = 4.7\text{ }\Omega$	—	52	—	ns
	Turn-off time		—	80	—	

Note: Pulse test

Switching Time Test Circuit

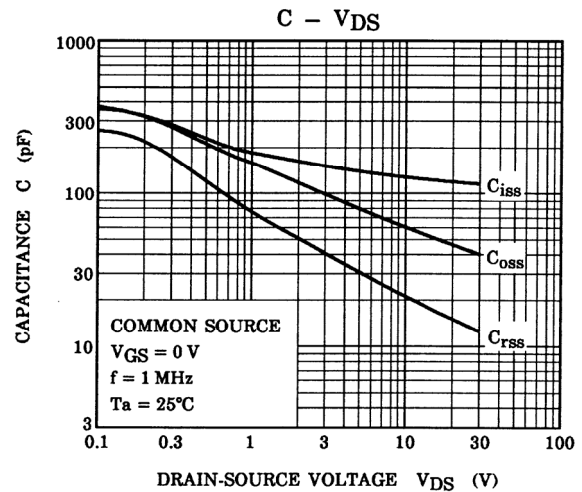
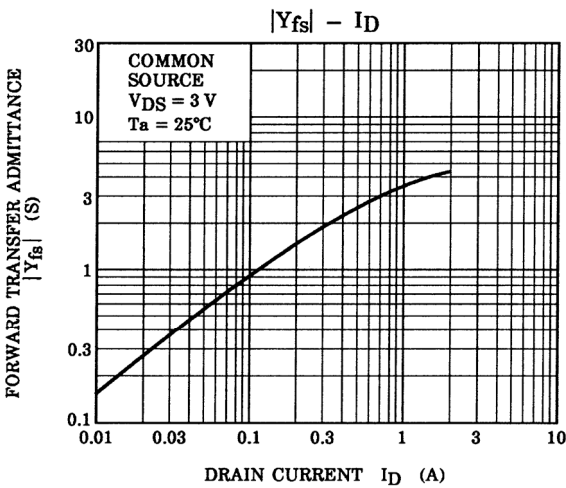
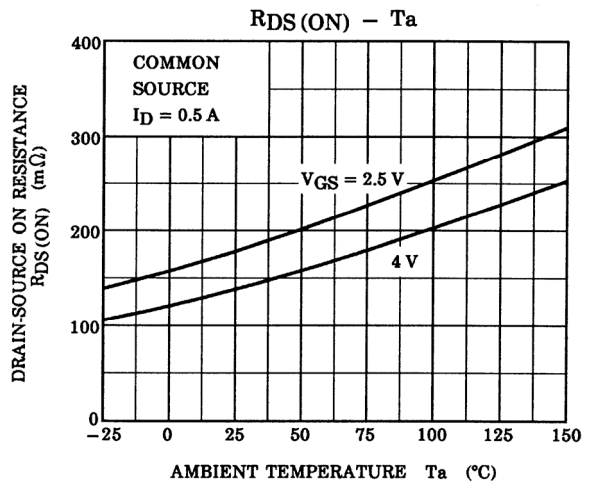
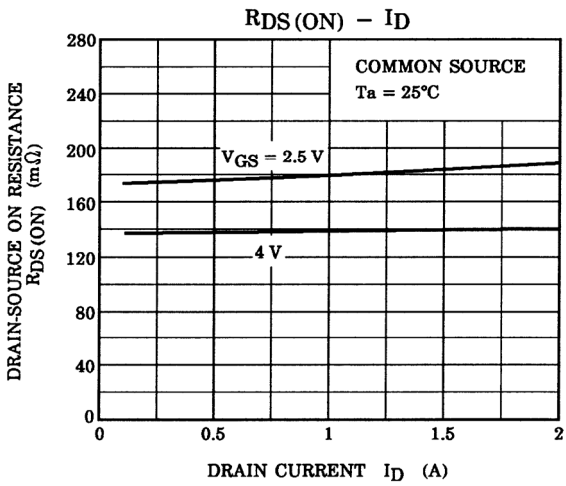
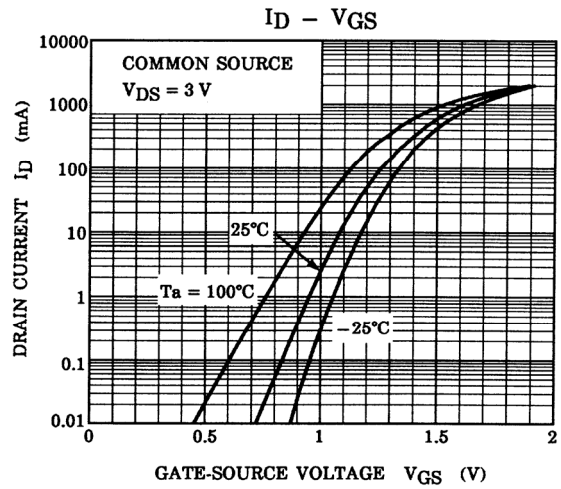
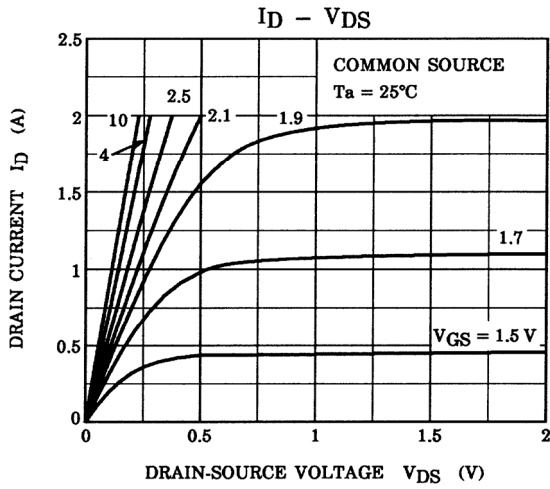


Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = 100\text{ }\mu\text{A}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires higher voltage than V_{th} and $V_{GS(off)}$ requires lower voltage than V_{th} .

(Relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(ON)}$)

Please take this into consideration for using the device.



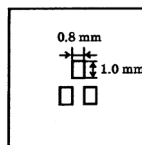
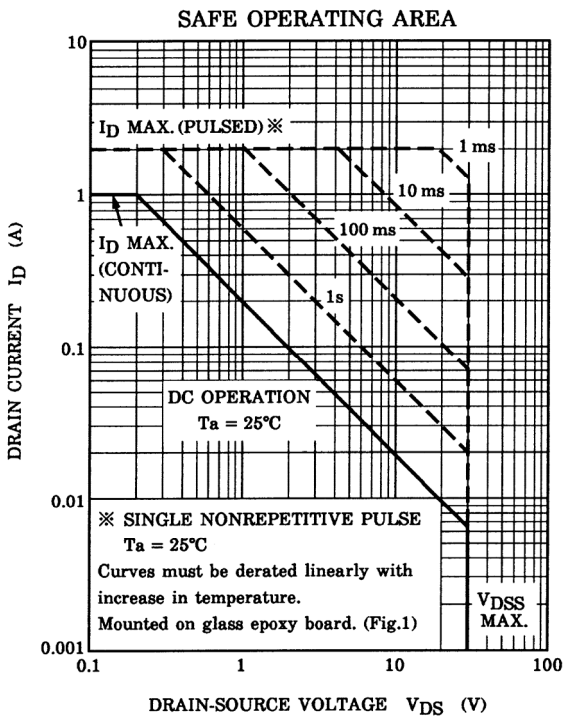
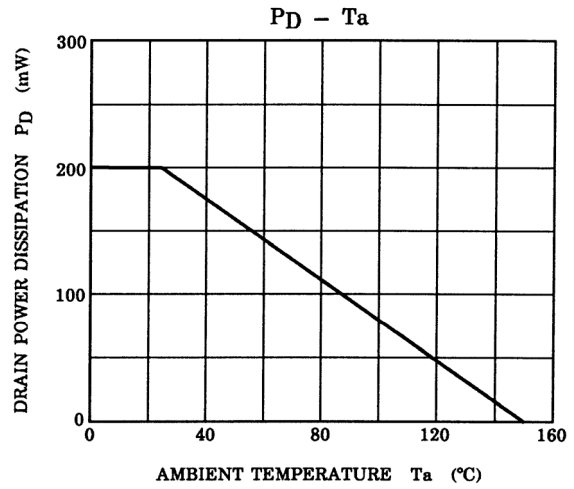
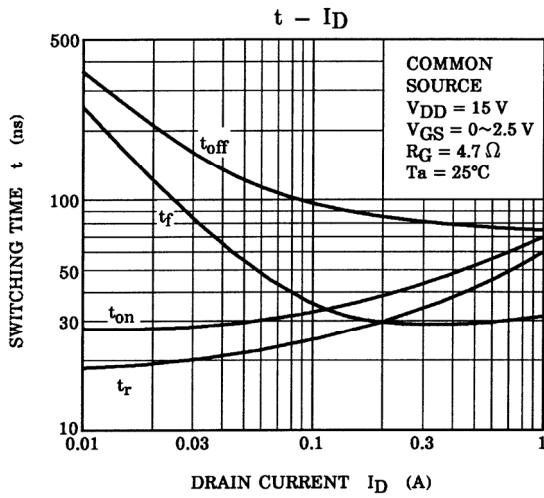


Figure 1 25.4 mm × 25.4 mm × 1.6 t (a Cu pad of 0.8 mm² area)

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20070701-EN GENERAL

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